(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 507 022 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **91303027.6**

(51) Int. Cl.5: **H04L 12/56**

(22) Date of filing: **05.04.91**

(43) Date of publication of application:
07.10.92 Bulletin 92/41

(84) Designated Contracting States:
BE DE DK ES FR GR IT LU NL SE

(71) Applicant: **GEC PLESSEY TELECOMMUNICATIONS LIMITED**
P.O. Box 53 Telephone Road
Coventry, CV3 1HJ(GB)

(72) Inventor: **Hall, Robert Mark**
2 Northwood Close, Bassett
Southampton, Hants(GB)

(74) Representative: **Waters, Jeffrey et al**
GEC Patent Department, GEC Marconi Limited, West Hanningfield Road
Great Baddow, Chelmsford, Essex CM2 8HN(GB)

(54) Method and apparatus for identifying valid cells in a redundant path combining unit of an asynchronous transfer mode switch.

(57) A method and apparatus is provided for identifying valid cells in a redundant path combining unit of an asynchronous transfer mode switch having duplicated switching planes. The method comprising the steps of:-

a) Identifying the plane from which came the last cell to be passed in respect of a particular call,

b) Checking that a sequence number associated with the cell is not one greater than that stored in a storage means,

c) Checking that the last cell to be passed on the particular call was from the same plane,

d) Checking if the cell is a duplicate of the last cell to arrive on this plane, and,

e) Passing the cell to an output store if (c) is true and (d) is not true and storing in the storage means the sequence number of the cell.

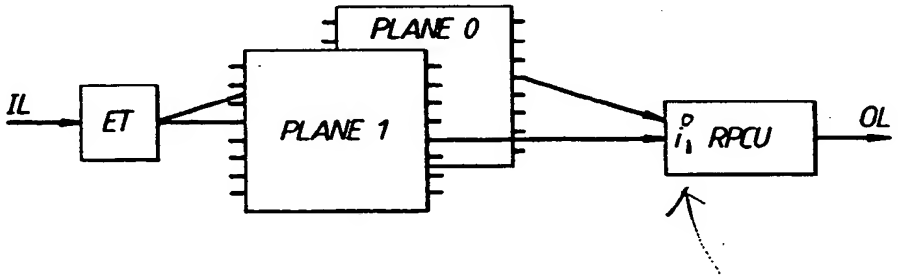

Fig.1.

EP 0 507 022 A1

The present invention relates to a method and apparatus for identifying valid cells in a redundant path combining unit of an asynchronous transfer mode switch having duplicated switching planes.

In a known type of validity checking apparatus, the redundant path combining unit is arranged to look at a sequence number attached to each data cell, to detect whether the sequence number matches that stored in a RAM or is greater by one. If either of these conditions are satisfied the cell is considered valid and the sequence number is incremented.

A disadvantage of this form of validity checking is that if the same two consecutive cells are lost from both planes, the redundant path combining unit would not allow any cells through until the sequence count had cycled round. For a 64 cell sequence follows:-

Plane 0 data	1, 2, 3, 4 ..... 63, 0, 1, 2
Plane 1 data	1, 2, 3, 4 ..... 63, 0, 1, 2

If cells 2 and 3, for example, are lost in both planes, then the following cells 4, 5, 6 ..... 63, 0, 1 are rejected in the cycle resulting in a total loss of 64 cells. This results in the needless prolongation of the original cell-loss error condition.

An object of the present invention is to provide a method and apparatus for identifying valid cells which does not suffer from the above mentioned disadvantage.

According to the present invention there is provided a method for identifying valid cells in a redundant path combining unit of an asynchronous transfer mode switch having duplicated switching planes, the method comprising the steps of:-

a) Identifying the plane from which came the last cell to be passed in respect of a particular call,

b) Checking that a sequence number associated with the cell is not one greater than that stored in a storage means,

c) Checking that the last cell to be passed on the particular call was from the same plane,

d) Checking if the cell is a duplicate of the last cell to arrive on this plane, and,

e) Passing the cell to an output store if (c) is true and (d) is not true and storing in the storage means the sequence number of the cell.

According to the present invention there is provided an apparatus for executing the method claimed in Claim 1, comprising transceiver means arranged to receive and transmit data, a first store connected to the transceiver means and, arranged to store plane identification data and cell sequence number data, a second store arranged to store a call identifier used to address the first store and a sequence number related to a particular call, for presentation to an addressed location in the first store, first comparator arranged to receive the sequence number from the second store and a sequence number from the first store and compare said numbers, a second comparator arranged to receive the sequence number from the second store, and the sequence number from the first store by way of an incrementer which is arranged to increment the sequence number by one, and compare said numbers, and cell acceptance logic circuitry connected to the first and second comparators and arranged to generate read and write control signals for the first store, in accordance with output signals generated by the first and second comparators.

An embodiment of the present invention will now be described with reference to the accompanying drawings in which:-

Figure 1 shows part of an asynchronous time mode switch incorporating duplicated switching planes, and,

Figure 2 shows part of the hardware incorporated in the redundant path combining unit necessary for executing the method.

Referring to Figure 1, an exchange termination unit ET has each incoming line IL connected to it. The data cells pertaining to a call, received on the line IL are passed to both switching planes P0 and P1 and are then switched to an output of the respective plane and passed to a redundant path checking unit RPCU. The redundant path checking unit RPCU receives therefore, a duplicate of each cell and it is arranged to decide whether the cells received from plane 0, P0 or plane 1, P1 should be passed to an outgoing line OL or discarded as a duplicate.

The redundant path checking unit RPCU achieves this by performing an algorithm. Each cell has an associated sequence number, enabling duplicate cells to be identified. The redundant path checking unit RPCU contains a look-up RAM 1 as shown in Figure 2, in which the sequence number is stored for each cell at an address which is identified by a virtual channel indicator VCI which is used to identify the call. The

VCI and sequence number are temporarily stored in a shift register 2. The VCI is used to address the RAM 1, and the next sequence number together with a plane identifier PI from which the last cell was accepted is written into the RAM under the control of cell acceptance logic circuitry 3. The sequence number is applied to first and second comparators 4, 5 which also receive from the RAM 1, the expected sequence number stored for the VCI indicator, and the plane identifier, PI.

The sequence number applied to the comparator 5 from the RAM 1, is incremented by one by circuit 6. The output signals from the comparators 4, 5 are applied to the cell acceptance logic circuitry 3 for controlling the read/write operation of the RAM 1.

The plane identifier PI is applied to the RAM 1 over line 7. The cell acceptance logic 3 also receives a RAM cycle start signal over line 8. The RAM 1 has data written to it, and read from it by a transceiver, TC and is controlled by a microprocessor.

An example of how cells could arrive at the redundant path checking unit RPCU is as follows:

1, 2, β, $\not{4}$, 5, 6 ..... Plane 0

1, 2, β, $\not{4}$, 5, 6 ..... Plane 1

The above represents the cell sequence for plane 0 and plane 1. Assuming that the cells shown crossed do not arrive at the redundant path checking unit RPCU because they are lost due to faults or errors, and cells 1 and 2 of plane 0 are accepted, cell 5 is valid but is out of sequence because the redundant path checking unit is expecting the sequence number of cell 3. Cells 1 and 2 of plane 1 are rejected as they would be duplicates of cells 1 and 2 accepted on plane 0.

The circuitry described above executes the following algorithm. The algorithm notes the plane from which came the last cell to be passed in respect of the particular VCI. If the cell arrives from e.g. plane 0 and the sequence number is not one greater than that held in the RAM 1, and two further checks are made as follows:-

1) Was the last cell to be passed on this VCI from this plane?

2) Is this cell a duplicate of the last cell to arrive on this plane? This can be detected as the sequence number of this cell being the same as that stored in the RAM 1.

If 1 is true and 2 is not true, then the cell is passed to an output FIFO in the transceiver and the sequence number stored in the RAM 1, is the sequence number of this cell.

The redundant path checking unit RPCU accepts a cell if the sequence number is the next in the sequence. The sequence number written back to the RAM 1 is that of the accepted cell.

The algorithm is shown below in pseudo code:-

```
BEGIN                          Plane-sent-bit: = 0;   (Set up variables)
                               Ram-seq-no: = 63;

When cell arrives on plane do Begin

Acceptance Loop                If cell-seq-no <> RAM-seq-no then Begin

Normal acceptance              If cell-seq-no = RAM-seq-no +1 then
                               Begin
                               Cell-accepted: = True;
                               RAM-seq-no: = cell-seq-no;
                               Plane-sent-bit: = This-plane;
```

```
                                    End;

Out of Sequence                     If Plane-sent-bit = This-plane then
                                    Begin
                                    Cell-accepted: = True;
                                    Out-of-sequence: = True;
                                    RAM-seq-no: = cell-seq-no;
                                    End;

End;  Else IF Plane-sent-bit = This-plane then
      Duplicate-cell-alarm: = True;

                  END.
      END.
```

Variables:		
	cell-seq-no	The sequence number of this incoming cell.
	RAM-seq-no	The sequence number held in RAM for this VCI.
	Plane-sent-bit	The Plane from which the last cell on this VCI was accepted.
	This-plane	The plane that this cell has come from (0 or 1).
	Cell-accepted	Control variable to say whether this cell is passed to the output FIFO.
	Duplicate-cell-alarm	Indication to microprocessor that a cell which is a duplicate of the last cell on this call on this plane has arrived.
	Out-of-sequence	Indication to microprocessor that cells have been lost i.e. the cell sent is out of sequence.

The algorithm does not cause a modulo 64 sequence loss to occur due to the situation described above with respect to the prior art, and the performance in other situations is equal to that of previously used algorithms.

Claims

1. A method for identifying valid cells in a redundant path combining unit of an asynchronous transfer mode switch having duplicated switching planes, the method comprising the steps of:-
   a) Identifying the plane from which came the last cell to be passed in respect of a particular call,
   b) Checking that a sequence number associated with the cell is not one greater than that stored in a storage means,
   c) Checking that the last cell to be passed on the particular call was from the same plane,
   d) Checking if the cell is a duplicate of the last cell to arrive on this plane, and,
   e) Passing the cell to an output store if (c) is true and (d) is not true and storing in the storage

means the sequence number of the cell.

2. Apparatus for executing the method claimed in Claim 1, comprising transceiver means arranged to receive and transmit data, a first store connected to the transceiver means and, arranged to store plane identification data and cell sequence number data, a second store arranged to store a call identifier used to address the first store and a sequence number related to a particular call, for presentation to an addressed location in the first store, first comparator arranged to receive the sequence number from the second store and a sequence number from the first store and compare said numbers, a second comparator arranged to receive the sequence number from the second store, and the sequence number from the first store by way of an incrementer which is arranged to increment the sequence number by one, and compare said numbers, and cell acceptance logic circuitry connected to the first and second comparators and arranged to generate read and write control signals for the first store, in accordance with output signals generated by the first and second comparators.

3. A method and apparatus for identifying valid cells in a redundant path checking unit of a transfer mode switch substantially as hereinbefore described.

4. Apparatus for identifying valid cells in a redundant path checking unit of a transfer mode switch substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

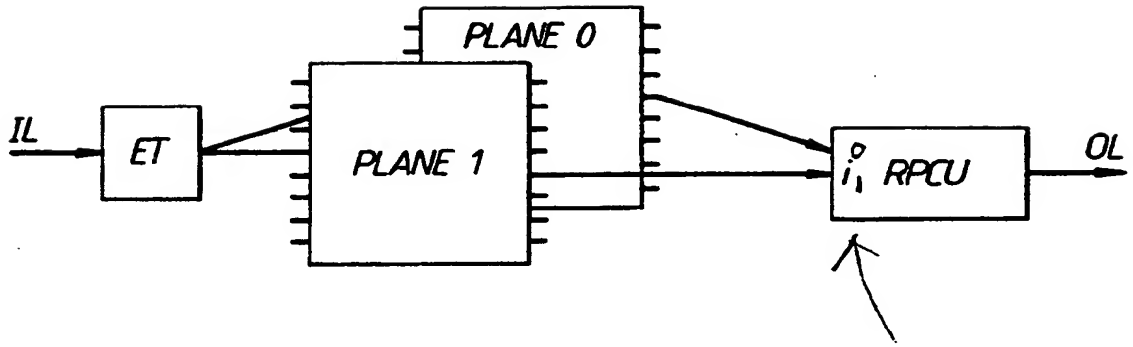

Fig.1.

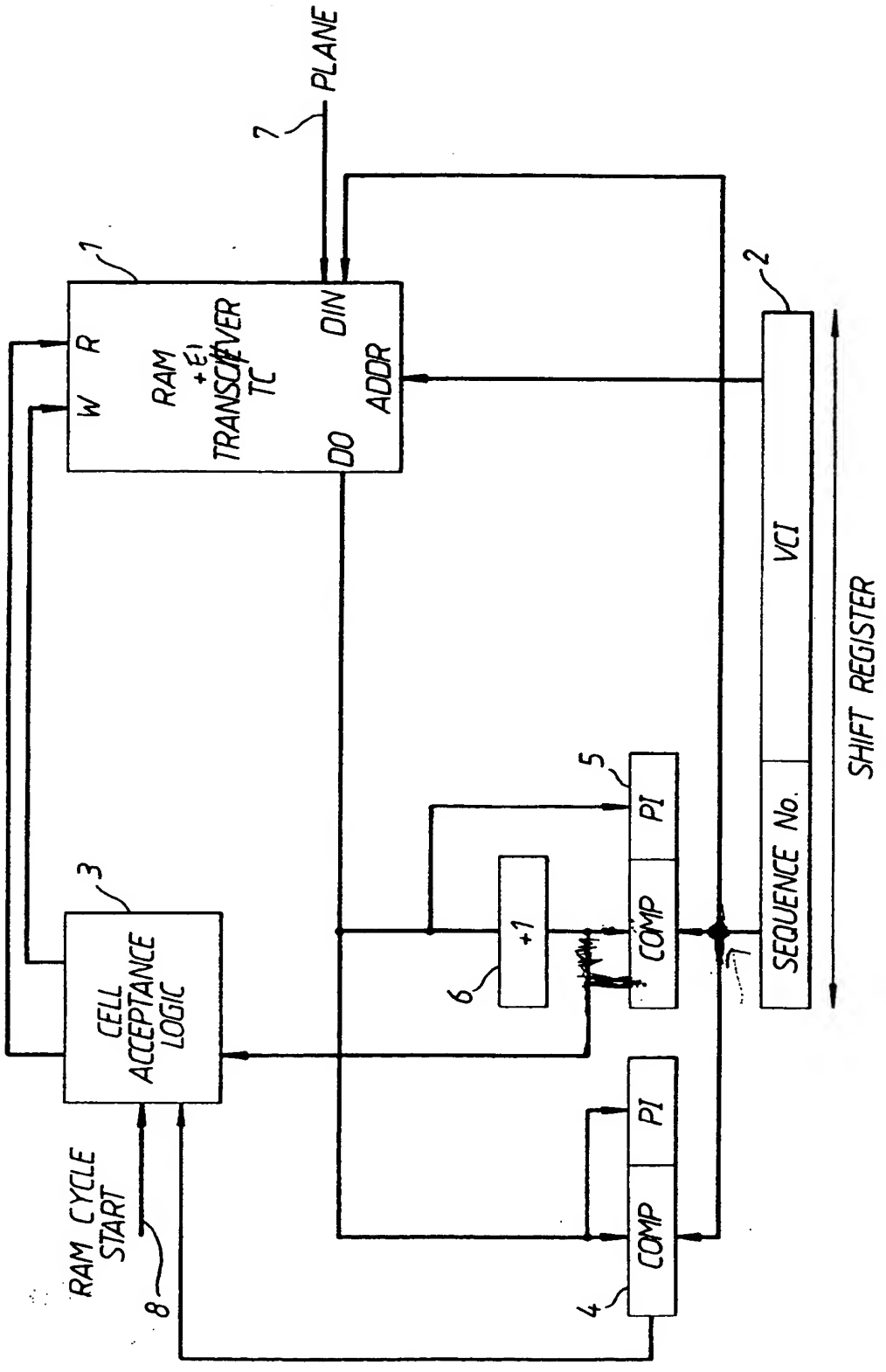
PLANE
7
1
RAM
+E1
TRANSCEIVER
TC
W
R
DIN
ADDR
DO
2
VCI
SEQUENCE No.
SHIFT REGISTER
3
CELL
ACCEPTANCE
LOGIC
5
PI
COMP
+1
6
4
PI
COMP
RAM CYCLE
START
8

Fig.2.

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 30 3027

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 384 936 (SIEMENS) * abstract * * colum 6, line 13 - colum 8, line 8 *	1,2	H04L12/56

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 OCTOBER 1991	C. MIKKELSEN

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)